HX3603 Preliminary Data Sheet v0.4

1 Product Definition

HX3603 is an ultra-low power Integrated AFE for Wearable, Optical, Heart-Rate Monitor and Bio-sensor.

2 Description

HX3603 is an ultra-low power integrated AFE for Wearable, Optical, Heart-Rate Monitor and Bio-sensor with I2C interface. HX3603 include transmitter and receiver two parts. The receiver have one PPG input channel, selectable TIA or Integrator, ±32uA offset IDAC and a high resolution ADC. The transmitter has three fully-integrated LED drivers with 3-bit current control. The device has a high dynamic range transmit and receive circuitry that helps with the sensing of very small signal.

3 Features

Accurate, Continuous Heart-Rate Monitoring:

1. Up to 100-dB dynamic range for accurate heart-rate detection
2. Support four phase data in each conversion period
4. Low power for continuous operation on a wearable device with a typical value:
   20 µA for an LED, 45 µA for the Receiver
   @ FS=25Hz， LED on time = 32uS , LED driver = 25mA

Transmitter:

1. 3 LEDs in common anode configurations
2. 3-Bit programmable LED current to 200 mA
3. Selectable LED on time
4. Simultaneous support of 3 LEDs for optimized SpO2, HRM, or multi-wavelength HRM
5. Average current of 20µA adequate for a typical heart-rate monitoring scenario:
   @ FS=25Hz, LED on time = 32uS, LED driver = 25mA

Receiver:

1. Supports 3 time-multiplexed PD inputs
2. 19-Bit representation of the current Input from a photodiode in unipolar straight binary format
3. Individual DC offset subtraction IDAC (Up to ±32µA) at TIA or integrator input for each phase
4. TIA mode resister range from 10K to 1.28M
5. Software sleep mode: approximately 0.5 µA current

Pulse Frequency: 1 SPS to 1000 SPS
FIFO With 16-Sample Depth
Pin-Selectable I2C Interface
Operating Temperature Range: -20℃ to 85℃
Supplies:

1. TX_SUP =3.0~4.2 V
2. VDDA =2.7~3.6 V

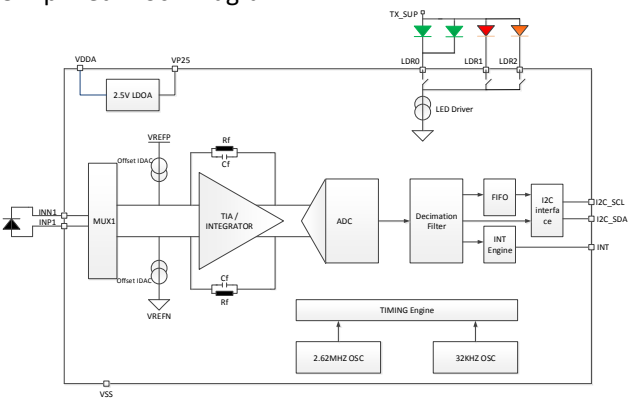
4 Applications

1. **Optical Heart-Rate Monitoring (HRM)**
2. **Heart-Rate Variability (HRV)**
3. **Pulse Oximetry (SpO2) Measurements**
4. **Maximum Oxygen Consumption (VO2 Max)**

5 PKG Information

3.0×3.0×0.75mm, 0.5mm pitch QFN16

Simplified Block Diagram



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6 Pin Configuration

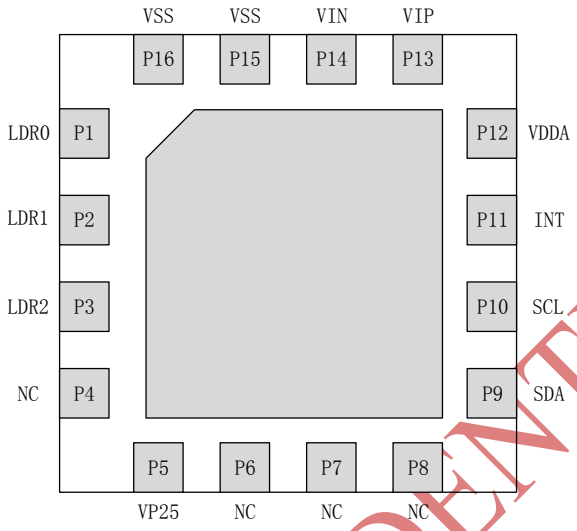


Figure 2 HX3603 TOP VIEW

6.1 PIN List

Pin	Name	Type	Description
1	LDR0	A	LED driver02, up to 200Ma
2	LDR1	A	LED driver02, up to 200Ma
3	LDR2	A	LED driver03, up to 200Ma
4	NC		
5	VP25	A	Internal 2.5V LDO output , need 1μF capacitor to GND
6	NC		
7	NC		
8	NC		
9	SDA	D	I2C data, external pull up resistor (for example, 10 kΩ)
10	SCL	D	I2C CLK, external pull up resistor (for example, 10 kΩ)
11	INT	D	CMOS output, ADC conversion ready interrupt signal and FIFO INT signal
12	VDDA	A	Power supply; 1μF capacitor to GND
13	VIP	A	External photo diode anode input pin
14	VIN	A	External photo diode cathode input pin
15	VSS	A	GND
16	VSS	A	GND

Table 1 HX3603 PIN list

7 Specifications

7.1 Absolute Maximum Rating(T_a=25℃, unless otherwise specified)

Parameter	Min	Max	Unit
VDDA to VSS	-0.3	4	V

Analog inputs	VDDA – 0.3	VDDA + 0.3	V
Digital inputs	VDDA – 0.3	VDDA + 0.3	V
Input current to any pin except supply pins		±7	mA
Operating temperature range	-20	85	℃
Maximum junction temperature		125	℃

7.2 Recommended Operating Conditions

	Min	Max	Unit
VDDA	2.6	3.6	V
TX_SUP	3.0	4.2	V
I2C_BUS_VOLTAGE	1.8	3.6	V
Supply voltage accuracy	±5		%
Specified temperature range	-20	85	℃
Maximum junction temperature		125	℃

7.3 ESD Ratings

		Value	Unit
V(esd) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±250	

7.4 Electrical Characteristics

Minimum and maximum specifications are at temperature = –20°C to 85°C, typical specifications are at 25°C. VDDA=3.3V, TX_SUP= 4V, 25Hz date output rate, LED driver current 25mA, led on time= 32uS, 32KHz and 2.62MHz internal clock, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY					
PRF(1) Pulse repetition frequency		1		1000	SPS
RECEIVER					
Offset cancellation DAC current range	7 bits IDAC		- 32 to 32		uA
Offset cancellation DAC current step			250		nA
TIA gain setting (Rf)	3 bits control		10k to 1.28M		Ω
Integrator gain setting (Cint)	4 bits control		3.125 to 50		pF
Integrator capacitor step			3.125		pF
TRANSMITTER					
LED current range			3.2 to 204.8		mA
LED current resolution			6		Bits
CLK (Internal 4MHz Oscillator , used to generate TIA and ADC timing)					
Frequency			2.62		MHz
Accuracy	Room temperature		±1%		
Frequency drift with temperature	Full temperature range		±0.5%		
CLK (Internal 32KHz Oscillator , used to generate PRF and INT timing)					
Frequency			32		KHz
Accuracy	Room temperature		±1%		
Frequency drift with temperature	Full temperature range		±0.5%		
I2C INTERFACE					
Maximum clock speed			800		KHz
I2C slave address			0x44		HEX
PERFORMANCE					

Receiver DR(dynamic range)		100	dB
Transmitter DR(dynamic range)		91	dB
CURRENT CONSUMPTION			
Receiver current	data conversion state	< 550	uA
	PRF wait state	< 40	uA
	Solftware sleep state	< 2	uA
TX LED current	Normal operation	20(2)	uA
	Solftware turnoff mode	< 0.1	uA
DIGITAL INPUTS			
V_{IH} High-level input voltage		0.9*VDDA VDDA	V
V_{IL} Low-level input voltage		0 0.1*VDDA	V
DIGITAL OUTPUTS			
V_{OH} High-level output voltage		VDDA	V
V_{OL} Low-level output voltage		0	V

(1) PRF refers to the rate at which samples from each of the three phases are output from the AFE.

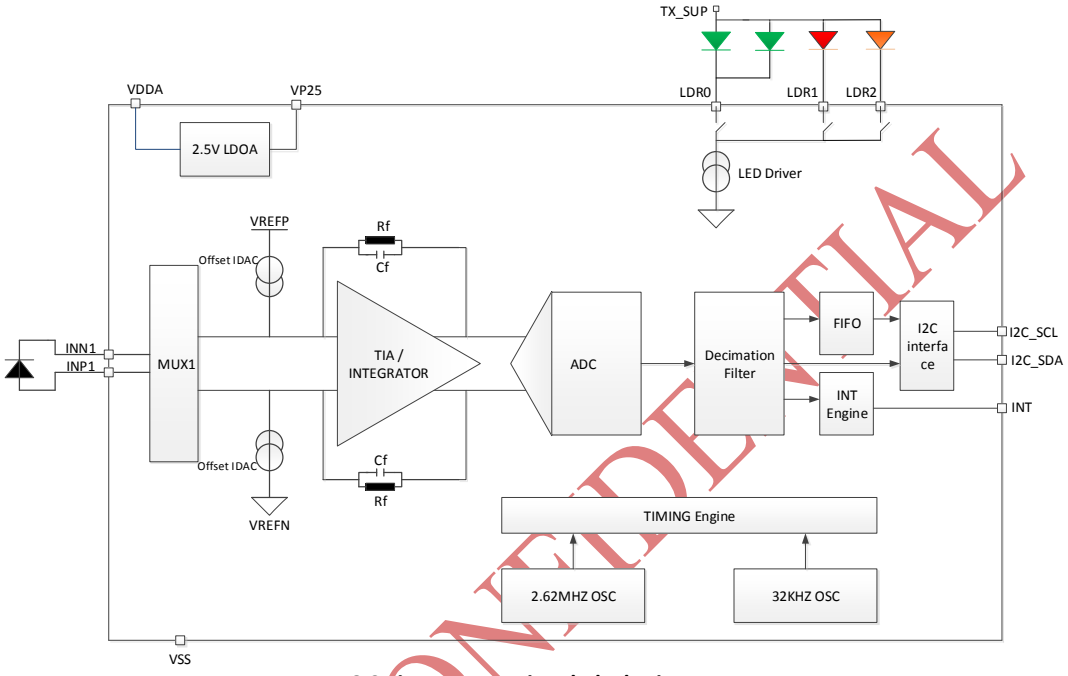
(2) I_tx = 25mA*32uS/40mS = 20uA

8 Detailed Description

8.1 Overview

The AFE has an integrated transmitter and receiver for optical heart-rate monitoring and pulse oximetry applications. The system is characterized by a parameter termed the pulse repetition frequency (PRF) that determines the repetition periodicity of a sequence of operations. Every cycle of a PRF results in four 19-bit digital samples at the output of the AFE, each of which is stored in a separate register.

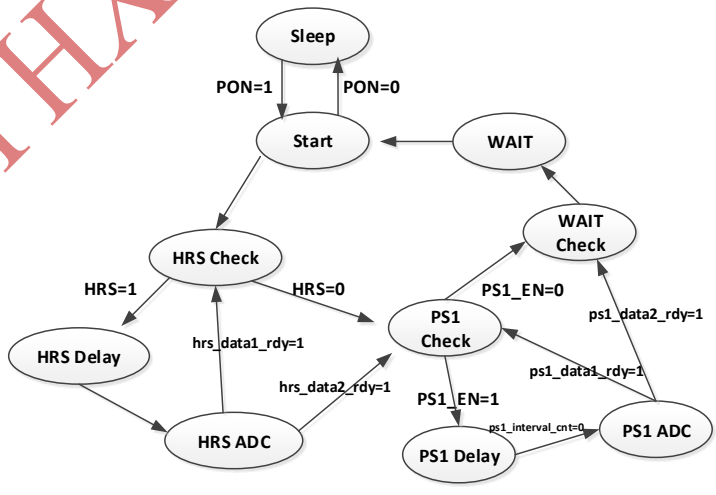
8.2 Functional Block Diagram



8.2 Figure1. Functional Block Diagram

8.3 Digital State Machine Diagram

The device has mainly three modes: 1 **sleep mode**, which configured by register SLEEP_EN, power consumption less than1uA. 2 **data conversion mode**. 3 **PRF wait mode**.



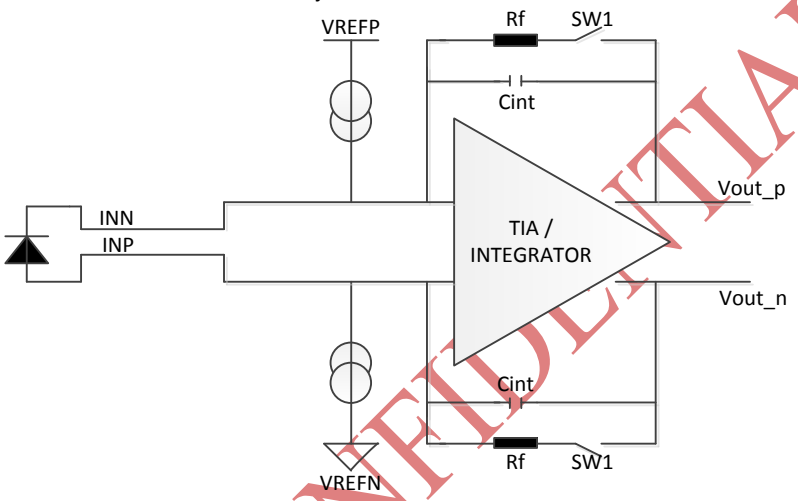
8.3 Figure1. Chip State machine diagram

8.4 Timing Diagram

The device works under two internal clocks, 32KHz system clock and2.62MHz AFE timing clock. 32KHz clock running all the time unless in chip sleep mode. It determine the PRF through register **0x10~0x11**. 2.62MHz high frequency clock only enabled in data conversion mode, and used to provide timing source for ADC and other high clock circuit.

8.5 TIA or Integrator

The receiver input pins (VIP, VIN) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a transimpedance amplifier (TIA, when SW1 close) or a Integrator(when SW1 open). The TIA gain is set by its feedback resistor (Rf) and can be programmed from 10 kΩ to 1 MΩ. The transimpedance gain between the input current and output differential voltage of the TIA is equal to 2×Rf. The Integrator gain is set by its integration capacitor (Cint) and can be programmed from 3.125pF to 50pF through register **0x0A**. The DC Offset IDAC current is used to cancellation DC part in signal. The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on power supplies.



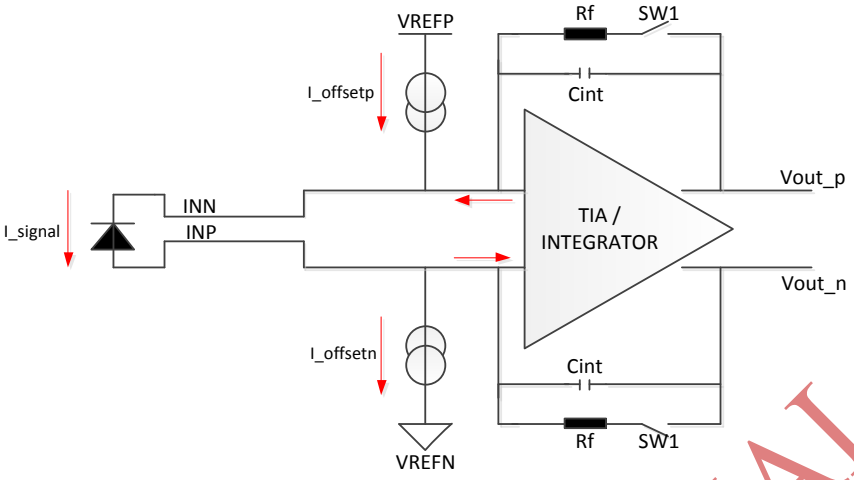
8.5 Figure1. PPG signal Input circuit

8.6 TIA or Integrator Setting

TIA MODE : VOUT = Vout_P – Vout_N = 2×(I_signal – I_offset) ×Rf;
Integrator MODE: VOUT = Vout_P – Vout_N = 2×(I_signal – I_offset) ×T_int×Cint;

8.7 Offset IDAC

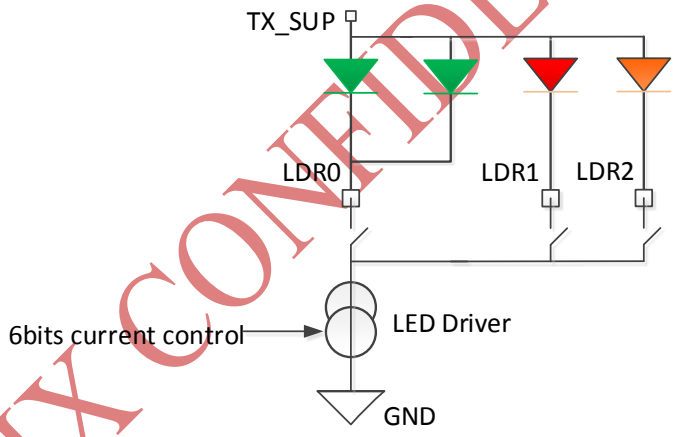
A typical optical heart-rate signal has a dc component and an ac component. Although a higher TIA or Integrator gain maximizes the ac signal at the AFE output, the magnitude of the dc component limits the maximum gain possible in the TIA. In order to decouple the affect of the dc level on the allowed ac signal gain, a current digital-to-analog converter (IDAC) is placed at the input of the device. By setting a programmable cancellation current (based on the dc current signal level), the effective signal that is gained up by the TIA can be reduced. In each of the three phases of operation. These cancellation currents are automatically presented to the input of the TIA in the appropriate phase. The ability to set a different cancellation current in each of the three phases can be used to cancel out the ambient current in the ambient phase. In the LED on phase, this ability can be used to cancel out the sum of the ambient current and dc current of the heart-rate signal.



8.7 Figure1. Offset IDAC

8.8 LED Driver

The device has one internal current DAC 3bits output current control. The output current control though register **0x0B<bit2:bit0>**for phase1 to phase3.



8.8 Figure1. LED driver circuit

8.9 Analog-to-Digital Converter (ADC)

The AFE has a two stage one bit sigma delta ADC that provides a largest 19-bit representation of the current from the photodiode. THE ADC has a configurable over sample rate(OSR) through register **0x01<bit1:bit0>/0x02< bit1:bit0>**. The ADC codes corresponding to the various sampling phases can be read out from 24-bit registers(**0XA0~0XAB**) in unipolar straight binary format. The ADC full-scale input range is ±1.8 V and spans bits 20 to 0. The mapping of the ADC input voltage to the ADC code is shown Table.

ADC over sample rate = 1024

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	24-BIT ADC OUTPUT CODE (Decimalism)
- 1.8V	0000 0000 0000 0000 0000 0000	0
0	0000 0100 0000 0000 0000 0000	262144
+1.8V	0000 0111 1111 1110 1111 1110	524030

ADC over sample rate = 512

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	24-BIT ADC OUTPUT CODE (Decimalism)
- 1.8V	0000 0000 0000 0000 0000 0000	0

0	0000 0000 1111 1110 0000 0001	65025
+1.8V	0000 0010 0000 0000 1011 1011	131259

ADC over sample rate = 256

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	24-BIT ADC OUTPUT CODE (Decimalism)
- 1.8V	0000 0000 0000 0000 0000 0000	0
0	0000 0000 0011 1111 1000 0000	16256
+1.8V	0000 0000 1000 0000 1000 0000	32896

ADC over sample rate = 128

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	24-BIT ADC OUTPUT CODE (Decimalism)
- 1.8V	0000 0000 0000 0000 0000 0000	0
0	0000 0000 0000 1111 1100 0000	4032
+1.8V	0000 0000 0010 0000 0100 0000	8256

9 Digital Interface

9.1 I2C

9.1.1 I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x44. The register index will automatically increase by 1 after the addressed register has been accessed (read or write).And the format is shown as following:

A Acknowledge (0)

P Stop Condition

R Read (1)

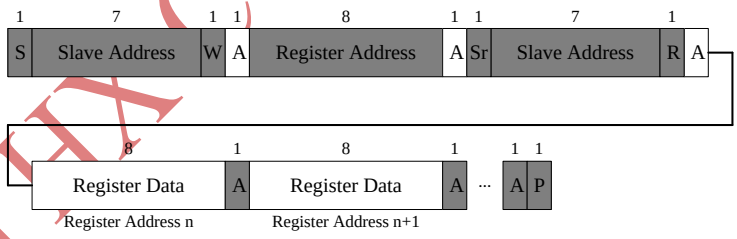
S Start Condition

W Write (0)

Sr Repeated Start Condition

■ Master-to- Slave
□ Slave-to-Master

I2C Write Register Data



I2C Read Register Data

Fig 9.1.1 I2C data format diagram

9.1.2 I2C AC Timing

Table1 Characteristics of the SDA and SCL I/O stages for F/S-mode I^2C-bus devices

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	0.5 0.5	1.5 0.3V_{DD}	n/a 0.5	n/a 0.3V_{DD} (1)	V V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	3.0 0.7V_{DD}	(2) (2)	n/a 0.7V_{DD}(1)	n/a (2)	V V
Hysteresis of Schmitt trigger inputs: V_{DD} > 2 V V_{DD} < 2 V	V_{hys}	n/a n/a	n/a n/a	0.05V_{DD} 0.1V_{DD}	– –	V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: V_{DD} > 2 V V_{DD} < 2 V	V_{OL1} V_{OL3}	0 n/a	0.4 n/a	0 0	0.4 0.2V_{DD}	V V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	–	250(4)	20 + 0.1C_b(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1V_{DD} and 0.9V_{DDmax}	I_i	10	10	10(5)	10(5)	A
Capacitance for each I/O pin	C_i		10		10	pF

Notes

1. Devices that use non-standard supply voltages which do not conform to the intended I^2C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum V_{IH} = V_{DDmax} + 0.5 V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 2 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off. n/a = not applicable

Table2 Characteristics of the SDA and SCL bus lines for F/S-mode I^2C-bus devices(1)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6		s
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	s
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	s
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	s
Data hold time	$t_{HD;DAT}$	0(2)	3.45(3)	0(2)	0.9(3)	s
Data set-up time	$t_{SU;DAT}$	250		100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	s
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	s
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 1).
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

n/a = not applicable

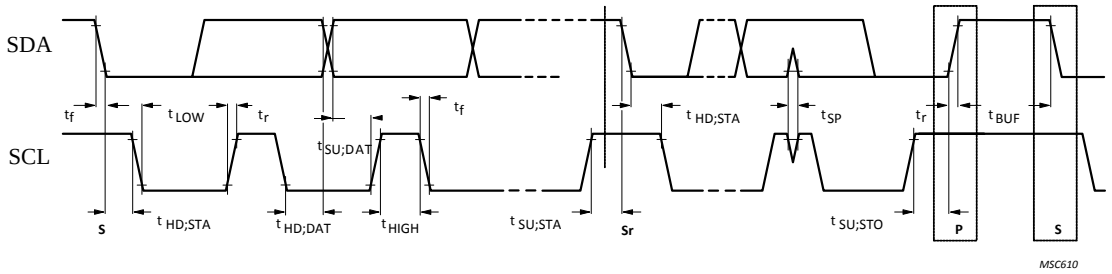


Fig 9.1.2 I2C Timing diagram

10 Application Information

A typical I2C interface application Schematic Diagram and Typical SPI Interface Application Schematic Diagram for HX3603 is shown in Figure 3 and Figure 4. The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistor (Rp). It is recommended use 10 kΩ resistor when running at 400kbps.

DEVICE NAME	Value	Description
LDO	2.7~3.6 V	Low noise
R1	22 Ω	
R2	10 KΩ	
R3	10 KΩ	
R4	10 KΩ	
C0	4.7 uF	
C1	1 uF	
C2	1 uF	

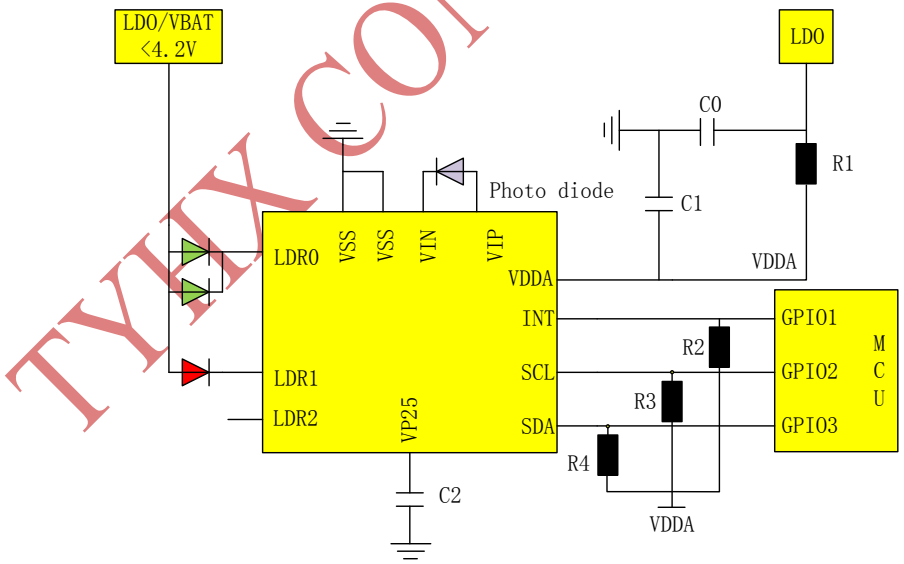
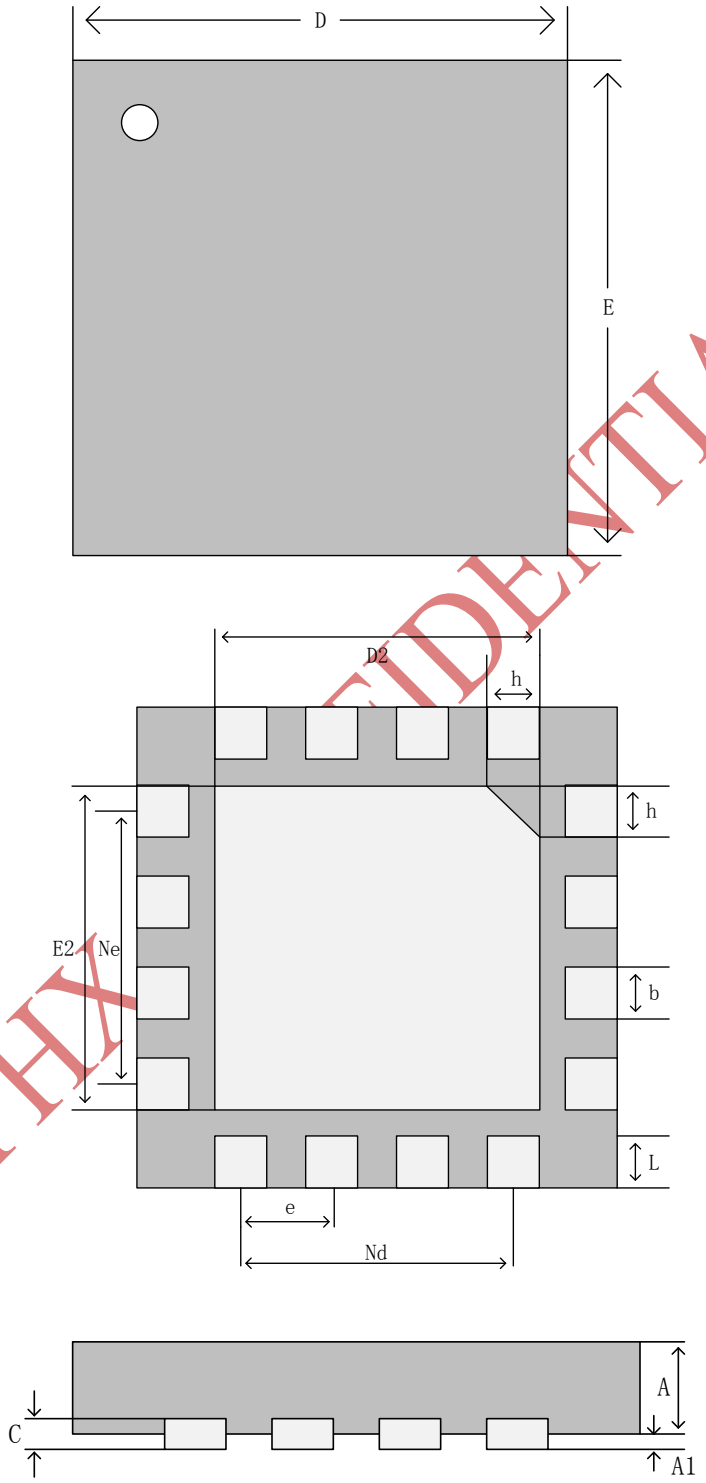


Figure 3 Typical I2C Interface Application Schematic Diagram

11 Package Information



SYMBOL	MILLIMETER		
	MIN	MON	MAX
A	0.65	0.75	0.85
A1		0.02	0.05
b	0.18	0.25	0.3
c	0.18	0.2	0.25
D	2.9	3	3.1
D2	1.55	1.65	1.75
e	0.5BSC		
Ne	1.5BSC		
Nd	1.5BSC		
E	2.9	3	3.1
E2	1.55	1.65	1.75
L	0.35	0.4	0.45
h	0.25	0.3	0.35

Figure 5 Package information

12 PCB Layout

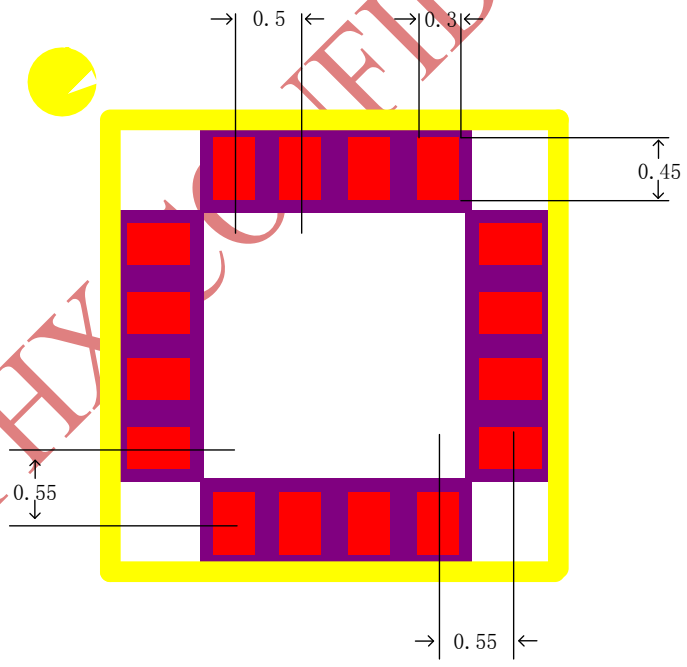


Figure 6 Mounting layout